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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,765	11/07/2001	Franck Roche	00RO30454288	9186

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/039,765	ROCHE ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-46 and 48-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-46 and 48-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 20-45 and 48-50 is withdrawn in view of the newly discovered reference(s) to SPI Block Guide, and System Management Bus (SMBus) Specification. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 20-43 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over SPI Block Guide(hereinafter referred to as SPI), in view of System Management Bus (SMBus) Specification(hereinafter referred to as SMB).

4. Regarding claim 20, SPI discloses a method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value(SCK=1), the method comprising: providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the device sending the data at least until

an instant when the clock line is released by the device to which the data is sent(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters.

5. Regarding claim 21, SPI discloses a method wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Figure 4-2).

6. Regarding claim 22, SPI discloses a method wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device(Figure 4-2, Data is applied before SCK Edge Nr. 1).

7. Regarding claim 23, SMB discloses a method wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Section 4.3.3, Figure 4-7).

8. Regarding claim 24, SMB discloses a method wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Page 22, Section 4.3.3, Figure 4-7).

9. Regarding claim 25, SPI discloses a method wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 4-2).

10. Regarding claim 26, SMB discloses a method wherein the slave device detects the second logic value on the clock line then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Section 4.3.3, Figure 4-7).

11. Regarding claim 27, SMB discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Section 4.3.3, Figure 4-7).

12. Regarding claim 28, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

13. Regarding claim 29, SMB discloses a method further comprising providing the slave device with a communication interface circuit including: trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value; an input for applying a clock line release signal to the trigger means; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger means and a second value when the clock line is released by the trigger means(Section 4.3.3, Figure 4-7).

14. Regarding claim 30, SPI discloses a method, wherein the communication interface circuit further comprises: means for storing at least one data; and means for automatically applying the

at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 4-3).

15. Regarding claim 31, SPI discloses a method, wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

16. Regarding claim 32, SPI discloses a method of transmitting data between two devices connected via a clock line and at least one data line, the method comprising: maintaining the clock line on a first logic value by default(SCK=1); providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters.

17. Regarding claim 33, SPI discloses a method, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic

value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Figure 4-2).

18. Regarding claim 34, SPI discloses a method, wherein the master device ties the clock line to the second logic value after applying data the data line when the master device is sending the data to the slave device(Figure 4-2, Data is applied before SCK Edge Nr. 1).

19. Regarding claim 35, SMB discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Section 4.3.3, Figure 4-7).

20. Regarding claim 36, SMB discloses a method, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Section 4.3.3, Figure 4-7).

21. Regarding claim 37, SPI discloses a method, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 4-2).

22. Regarding claim 38, SMB discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Section 4.3.3, Figure 4-7).

23. Regarding claim 39, SMB discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master

device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Section 4.3.3, Figure 4-7).

24. Regarding claim 40, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

25. Regarding claim 41, SMB discloses a method providing the slave device with further a communication comprising interface circuit including: a trigger circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value; an input for applying a clock line release signal the trigger circuit; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger circuit and a second value when the clock line is released by the trigger circuit(Section 4.3.3, Figure 4-7).

26. Regarding claim 42, SPI discloses a method wherein the communication interface circuit further comprises: a buffer for storing at least one data; and a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 4-3).

27. Regarding claim 43, SPI discloses a method wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

28. Regarding claim 48, SPI discloses a synchronous data transmission system comprising: a clock line; a data line; a master data transmitting/receiving comprising a clock line connection terminal for connection to a clock line; at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); means for tying the clock line to a potential representing a

second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); and data sending means for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent(Figure 4-2) and a slave data transmitting/receiving comprising a clock line connection terminal connected to the clock line; at least one data line connection terminal connected to the data line and means for detecting a change from the first logic value to the second logic value on the clock line, and reading the data on the data line, when the data is to be received(Figure 4-2).

SPI does not specifically disclose means for tying the clock line to the potential representing the second logic value. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have a slave hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters.

29. Regarding claim 49, SPI discloses a system, wherein the master device further comprises data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received by the master device(Figure 4-2).

30. Regarding claim 50, SMB discloses a system, wherein the slave device further comprises means for detecting a change from the first logic value to the second logic value on the clock

line, tying the clock line the second logic value, applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device(Page 22, Section 4.3.3, Figure 4-7).

Claim Rejections - 35 USC § 102

31. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

32. Claims 44-46 are rejected under 35 U.S.C. 102(a) as being anticipated by SPI.

33. Regarding claim 44, SPI discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line; at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); and data sending means for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent(Figure 4-2).

34. Regarding claim 45, SPI discloses a device, further comprising data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received(Figure 4-2).

35. Regarding claim 46, SPI discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line, the clock line being maintained by default on a first logic value(SCK=1); at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); means for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, and reading data on the data line, and releasing the clock line, if data is to be received(Figure 4-2), or applying data to the data line, and releasing the clock line if the data is to be sent(Figure 4-2, Data is applied before SCK Edge Nr. 1).

36. Claims 51 and 52 are rejected under 35 U.S.C. 102(a) as being anticipated by SMB.

37. Regarding claim 51, SMB discloses a communication interface circuit for connection to a data transmitting/receiving device via a clock line and at least one data line, the circuit comprising: means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value; trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value; an input to apply a clock line release signal to the trigger means; and an output to deliver an information signal that has a first value when the clock line is tied to the second logic signal by the trigger means and a second value when the clock line is released by the trigger means(Page 22, Section 4.3.3, Figure 4-8).

38. Regarding claim 52, SMB discloses a communication interface circuit further comprising: means for storing data; and means for automatically applying the data to the data

line when the clock line changes from the first logic value to the second logic value(Section 4.3.3, Figure 4-7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nimesh G Patel
Examiner
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NP
April 14, 2007

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